IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SAN et al.

Atty. Ref.: 1248-29

Serial No. Cont. of S.N. 09/725,561
(filed November 30, 2000)

Group: Unassigned

Filed: Herewith

Examiner: Unassigned

For: EXTERNAL MEMORY SYSTEM HAVING PROGRAMMABLE GRAPHICS PROCESSOR FOR USE IN A VIDEO GAME SYSTEM OR THE LIKE

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May 15, 2001

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

In order to place the above-identified application in better condition for examination, please amend the application as follows:

In The Specification:

On page 1, before the first line, please insert the following written paragraph:

--This is a continuation of application Serial No. 09/725,561, filed November 30, 2000, which in turn is a continuation of application Serial No. 08/920,871, filed August 29, 1997 (now abandoned), which in turn is a division of application Serial No. 08/385,160, filed February 7, 1995, which in turn is a division of application Serial No. 07/827,098, filed January 30, 1992 (now U.S. Patent No. 5,388,841)--.

Please replace the paragraph beginning at line 16 of page 1 with the following rewritten paragraph:

--This application is related to application Serial No. 08/337,142, filed November 10, 1994, which is a continuation of Serial No. 07/827,201 by San et al, entitled "Programmable Graphics Processor Having Pixel To Character Conversion Hardware For Use In A Video Game System Or The Like" and U.S. Patent No. 5,357,604, issued October 18, 1994 by San et al, entitled "Graphics Processor with Enhanced Memory Control Circuitry For Use In a Video Game System Or The Like".--

Please replace the paragraph beginning at line 23 of page 9 with the following rewritten paragraph:

--In addition to the read buffering feature which is initiated upon any access to register R14 as described above, the graphics coprocessor of the present invention also includes write buffering features in which data to be written to the game cartridge RAM is buffered to enable the central processing unit of the graphics coprocessor to execute other instructions as rapidly as possible.--

Please replace the paragraph beginning at line 3 of page 16 with the following rewritten paragraph:

--In accordance with the present exemplary embodiment, the graphics coprocessor of the present invention interacts with a 16-bit video game system commercially sold by Nintendo of America, Inc. as the Super Nintendo Entertainment System (Super NES). The Super Nintendo Entertainment System is described in part in U.S. Patent No. 5,327,158, issued July 5, 1994, entitled "Video Processing Apparatus" and U.S. Patent No. 5,291,189, issued March 1, 1994, entitled "Direct Memory Access Apparatus and External Storage Device Used Therein". These

patents are expressly incorporated herein by reference. It should be understood that the present invention is not limited to Super NES related applications and may be used with other video game systems or other, non-video game, information processing apparatus.--

Please replace the paragraph beginning at line 7 of page 26 with the following rewritten paragraph:

--Since the ROM 10 and RAM 6, 8 on the cartridge are on separate buses, they can be accessed in parallel by the Mario Chip. Also RAMs 6, 8 can be accessed at a faster rate than ROM and the Mario chip is designed to utilize this performance advantage. The Mario chip has no access to any memory that is inside the Super NES, i.e., no access to the working RAM 32 or PPU video RAM 30.--

Please replace the paragraph beginning at line 24, of page 28 through line 12 of page 29 with the following rewritten paragraph:

--The Super NES video game machine which is represented in block form in Figure 2 has only been generally described herein. Further details regarding the Super NES including PPU 24 may, for example, be found in U.S. Patent No. 5,327,158, issued July 5, 1994, entitled "Video Processing Apparatus, which patent has been expressly incorporated herein by reference. Still further details such as how information is transferred between the Super NES and the game cartridge may be found in U.S. Patent No. 5,291,189, issued March 1, 1994, entitled "Direct Memory Access Apparatus in Image Processing System and External Storage Device Used Therein" and in U.S. Application Serial No. 07/793,735, filed November 19, 1991, entitled, "Mosaic Picture Display Apparatus and External Storage Unit Used Therefor", which applications are incorporated herein by reference.--

Please replace the paragraph beginning at line 22 of page 29 through line 4 of page 30 with the following rewritten paragraph:

--Figure 3 shows a perspective view of an exemplary mechanical design for a game cartridge case 19 for housing the Mario chip and other cartridge structure shown in Figure 1. Similarly, Figure 3 shows the perspective view of an exemplary exterior housing for a video game control deck 20 for housing the Super NES video game hardware shown in Figure 2. The mechanical design for such video game control deck 20 and associated removable game cartridge 19 is shown in Figures 2-9 of U.S. Patent No. 5,192,082, issued on March 9, 1993, entitled, "TV Game Machine", which patent is hereby incorporated herein by reference.--

In The Abstract:

Please delete the originally-filed Abstract and substitute in its place the Abstract found on a separate sheet attached at the end of this amendment.

In The Claims:

Please cancel claims 1-79, without prejudice or disclaimer.

Please add the following claims 80-205.

--80. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising:

a programmable graphics processor;

a main processor that communicates information relating to one or more polygon-based 3D graphic objects to said programmable graphics processor,

wherein the graphics processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device.

81. A home video game system as in claim 80 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

82. A home video game system as in claim 80 wherein the graphics processor is a pipelined processor.

83. A home video game system as in claim 80 wherein the graphics processor is a programmable pipelined processor.

84. A home video game system as in claim 80 wherein the graphics processor includes embedded RAM cache memory.

85. A home video game system as in claim 80 wherein the graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

86. A home video game system as in claim 80 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

87. A home video game system as set forth in claim 86 wherein the multiplier performs multiply operations using at least 16-bit length operands.

88. A home video game system as in claim 80 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

89. A home video game system as in claim 80 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

90. A home video game system as in claim 80 wherein the graphics processor is programmed to perform texture mapping operations.

91. A home video game system as in claim 80 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

92. A home video game system as in claim 80 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

93. A home video game system as in claim 80 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

94. A home video game system as in claim 80 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

95. A home video game system as in claim 80 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

96. A home video game system as in claim 80 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

97. A home video game system as in claim 80 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

98. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving removable memory, comprising:

a game program processing unit for executing at least a portion of a videographics program for displaying polygon-based 3D objects; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for rendering one or more portions of polygon-based 3D objects for display on said television type monitor display.

99. A home video game system as in claim 98 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

100. A home video game system as in claim 98 wherein the graphics processor is a pipelined processor.

101. A home video game system as in claim 98 wherein the graphics processor includes a high speed multiplier circuit.

102. A home video game system as in claim 98 wherein the graphics processor includes embedded RAM cache memory.

103. A home video game system as in claim 98 wherein the graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

104. A home video game system as in claim 98 wherein the graphics processor includes at least an Arithmetic Logic Unit and a plurality of registers for executing instructions for performing rotation and/or scaling of a polygon-based graphic object to be displayed.

105. A home video game system as in claim 98 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

106. A home video game system as set forth in claim 105 wherein the multiplier performs multiply operations using at least 16-bit length operands.

107. A home video game system as in claim 98 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

108. A home video game system as in claim 98 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

109. A home video game system as in claim 98 wherein the graphics processor is programmed to perform texture mapping operations.

110. A home video game system as in claim 98 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

111. A home video game system as in claim 98 having a set of instructions for programming the graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

112. A home video game system as in claim 98 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed

multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

113. A home video game system as in claim 98 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

114. A home video game system as in claim 98 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

115. A home video game system as in claim 98 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

116. A home video game system as in claim 98 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

117. A home video game system for use with a television type display device said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data, comprising:

a game program processor; and

a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, said graphics processor including a programmable processor having embedded RAM cache memory.

118. A home video game system as in claim 117 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

119. A home video game system as in claim 117 wherein the graphics processor is a pipelined processor.

120. A home video game system as in claim 117 wherein the graphics processor includes a high speed multiplier circuit.

121. A home video game system as in claim 117 wherein the graphics processor includes a plurality of data storage registers.

122. A home video game system as in claim 117 wherein the graphics processor includes graphic geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

123. A home video game system as in claim 122 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

124. A home video game system as set forth in claim 123 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

125. A home video game system as in claim 117 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

126. A home video game system as in claim 117 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

127. A home video game system as in claim 117 wherein the graphics processor is programmed to perform texture mapping operations.

128. A home video game system as in claim 117 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

129. A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

130. A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

131. A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

132. A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

133. A home video game system as in claim 117 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

134. A home video game system as in claim 117 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

135. A home video game system, for use with a television type monitor display device, said system having a housing and an insertion port in the housing for receiving removable program memory, comprising:

a game program processing unit for executing at least a portion of a videographics program for displaying polygon-based 3D graphic objects;

a video RAM for providing video frame data to a display device; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for subsequent transfer to said video RAM corresponding to one or more portions of polygon-based objects to be displayed.

136. A home video game system as in claim 135 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

137. A home video game system as in claim 135 wherein the graphics processor is a pipelined processor.

138. A home video game system as in claim 135 wherein the transfer of pixel data to video RAM is a direct memory assess (DMA) type transfer.

139. A home video game system as in claim 135 wherein the graphics processor includes a high speed multiplier circuit.

140. A home video game system as in claim 135 wherein the graphics processor includes embedded RAM cache memory.

141. A home video game system as in claim 135 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

142. A home video game system as in claim 135 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

143. A home video game system as set forth in claim 142 wherein the multiplier performs multiply operations using at least 16-bit length operands.

144. A home video game system as in claim 135 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

145. A home video game system as in claim 135 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

146. A home video game system as in claim 135 wherein the graphics processor is programmed to perform texture mapping operations.

147. A home video game system as in claim 135 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

148. A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

149. A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

150. A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

151. A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

152. A home video game system as in claim 135 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

153. A home video game system as in claim 135 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

154. A home video game system for use with a television type monitor display device comprising:

a housing including an insertion port that receives a removable memory storing video game program data/instructions;

a game program processor that executes at least a portion of a videographics game program which displays polygon-based 3D objects; and

a graphics processor that renders at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, the graphics processor including at least an Arithmetic Logic Unit and graphics geometry transformation circuitry for performing graphic transformation operations.

155. A home video game system as in claim 154 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

156. A home video game system as in claim 154 wherein the graphics processor is a pipelined processor.

157. A home video game system as in claim 154 wherein the graphics processor is a programmable pipelined processor.

158. A home video game system as in claim 154 wherein the graphics processor includes embedded RAM cache memory.

159. A home video game system as in claim 154 wherein the circuitry for accelerating 3D graphic special transformation operations includes a high speed multiplier for performing computations for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

160. A home video game system as in claim 154 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

161. A home video game system as set forth in claim 160 wherein the multiplier performs multiply operations using at least 16-bit length operands.

162. A home video game system as in claim 154 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

163. A home video game system as in claim 154 wherein two or more polygon-based graphic objects are displayed simultaneously.

164. A home video game system as in claim 154 wherein the graphics processor is programmed to perform texture mapping operations.

165. A home video game system as in claim 154 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

166. A home video game system as in claim 154 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

167. A home video game system as in claim 154 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

168. A home video game system as in claim 154 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

169. A home video game system as in claim 154 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

170. A home video game system as in claim 154 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

171. A home video game system as in claim 170 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

172. A home video game system for use with a television type monitor display device, said system having a housing and an insertion port in the housing for receiving removable

memory and including a game program processor and a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, the graphics processor comprising:

a programmable pipelined processor having an Arithmetic Logic Unit;

a multiplier unit;

a cache RAM; and

a plurality of registers;

wherein the graphics processor performs at least rotation and/or scaling operations on said polygon based objects.

173. A home video game system as in claim 172 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

174. A home video game system as in claim 172 wherein the graphics processor includes hardware geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

175. A home video game system as set forth in claim 172 wherein the multiplier performs multiply operations using at least 16-bit length operands.

176. A home video game system as in claim 172 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

177. A home video game system as in claim 172 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

178. A home video game system as in claim 172 wherein the graphics processor is programmed to perform texture mapping operations.

179. A home video game system as in claim 172 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

180. A home video game system as in claim 172 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

181. A home video game system as in claim 172 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

182. A home video game system as in claim 172 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

183. A home video game system as in claim 172 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

184. A home video game system as in claim 172 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

185. A home video game system as in claim 184 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

186. In a home video game system having a housing and an insertion port in the housing for receiving a removable memory for storing a video game program, said system including a

game program processor for executing at least a portion of a videographics program for displaying polygon-based 3D objects, a programmable graphics processor and a video RAM for providing video frame data to a television type monitor display device, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on the display device, comprising the steps of:

computing display screen position coordinates for a rotated and/or scaled polygon-based object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object to the video RAM.

187. A home video game system for use with a television type monitor display device, said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data, comprising:

a game program processor;

a graphics processor for rendering at least one or more portioning of a polygon-based 3D graphic object for displaying on the display device; and

a CD ROM reader device, wherein at least a portion of program instructions and/or graphics data used in rendering a 3D graphic object is accessed from a CD ROM.

188. A home video game system as in claim 187 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

189. A home video game system as in claim 187 wherein the graphics processor is a pipelined processor.

190. A home video game system as in claim 187 wherein the graphics processor includes a high speed multiplier circuit.

191. A home video game system as in claim 187 wherein the graphics processor includes a plurality of data storage registers.

192. A home video game system as in claim 187 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

193. A home video game system as in claim 192 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

194. A home video game system as set forth in claim 193 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

195. A home video game system as in claim 187 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

196. A home video game system as in claim 187 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

197. A home video game system as in claim 187 wherein the graphics processor is programmed to perform texture mapping operations.

198. A home video game system as in claim 187 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

199. A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

200. A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

201. A home video game system as in claim 187 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

202. In a home video game system having an insertion port for receiving removable memory for storing video game program data and/or instructions, said system including a game program processor and a programmable pipelined graphics processor, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on a raster scan type display device, comprising the steps of:

computing bit mapped display screen position object coordinates for a rotated and/or scaled polygon-based an object to be displayed; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object a video display RAM.

203. The method as in claim 202 wherein the writing of pixel information is accomplished via a direct memory access (DMA) operation.

204. In a home video game system, having a game program processor and a programmable graphics processor, the graphics processor having circuitry for increasing computational speed when processing 3D graphic geometric transformation operations, a method of producing 3D type graphics display effects utilizing rotated and/or scaled polygon-based objects, comprising the steps of:

providing said graphics processor with information relating at least in part to a polygon based graphic object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object a video display RAM.

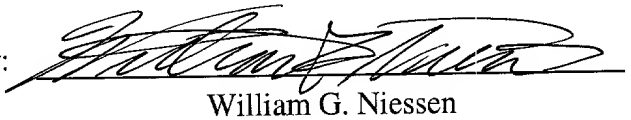
205. The method as in claim 204 wherein the writing of pixel information is accomplished via a DMA operation.--

REMARKS

Attached hereto is a replacement amended abstract of the disclosure and a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "Abstract of the Disclosure" and "Version With Markings To Show Changes Made."

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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ABSTRACT OF THE DISCLOSURE

A fully user-programmable, graphics processor is disclosed which is designed to be embodied in a removable external memory unit for connection with a host video game information processing system. In an exemplary embodiment, a video game system is described including a host video game system housing a game program processor and a pluggable video game cartridge containing the graphics processor. The graphics processor communicates with the host game processor and incorporates an embedded RAM cache memory. The programmable graphics processor has hardware circuitry for performing 3D geometry transformations such as rotating and/or scaling polygon-based 3D graphic objects and also includes dedicated hardware for plotting individual pixels for use with a character-mapped type display arrangement. The graphics processor utilizes an instruction set that is designed to efficiently implement rotation and scaling operations associated with 3D graphics and includes special instructions for plotting character-mapped pixels.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 1, before the first line, the following paragraph was inserted:

This is a continuation of application Serial No. 09/725,561, filed November 30, 2000, which in turn is a continuation of application Serial No. 08/920,871, filed August 29, 1997 (now abandoned), which in turn is a division of application Serial No. 08/385,160, filed February 7, 1995, which in turn is a division of application Serial No. 07/827,098, filed January 30, 1992 (now U.S. Patent No. 5,388,841).

The paragraph beginning at line 16 of page 1 has been amended as follows:

This application is related to [the currently filed] application Serial No. [___,___] 08/337,142, filed November 10, 1994, which is a continuation of Serial No. 07/827,201 by San et al, entitled "Programmable Graphics Processor Having Pixel To Character Conversion Hardware For Use In A Video Game System Or The Like" [Atty. Docket No. 1248-4).] and [concurrently filed application Serial No. ___,___] U.S. Patent No. 5,357,604, issued October 18, 1994 by San et al, entitled "Graphics Processor with Enhanced Memory Control Circuitry For Use In a Video Game System Or The Like" [(Atty. Docket No. 1248-5)].

The paragraph beginning at line 23 of page 9 has been amended as follows:

In addition to the read buffering feature which is initiated upon any access to register R14 as described above, the graphics coprocessor of the present invention also includes write buffering features in which data to be written to the game cartridge RAM is buffered to enable the central processing unit of the [Mario chip] graphics coprocessor to execute other instructions as rapidly as possible.

The paragraph beginning at line 9, of page 16 has been amended as follows:

In accordance with the present exemplary embodiment, the graphics coprocessor of the present invention interacts with a 16-bit video game system commercially sold by Nintendo of America, Inc. as the Super Nintendo Entertainment System (Super NES). The Super Nintendo Entertainment System is described in part in U.S. [application Serial No. 07/651,265] Patent No. 5,327,158, issued July 5, 1994, entitled "Video Processing Apparatus" [which was filed on April 10, 1991] and U.S. [application Serial No. 07/749,530, filed on August 26, 1991] Patent No. 5,291,189, issued March 1, 1994, entitled "Direct Memory Access Apparatus and External Storage Device Used Therein". These [applications] patents are expressly incorporated herein by reference. It should be understood that the present invention is not limited to Super NES related applications and may be used with other video game systems or other, non-video game, information processing apparatus.

The paragraph beginning at line 8 of page 26 has been amended as follows:

Since the ROM 10 and RAM 6, 8 on the cartridge are on separate buses, they can be accessed in parallel by the Mario Chip. Also RAMs 6, 8 can be accessed at a faster rate than ROM and the Mario chip is designed to utilize this performance advantage. The Mario chip has no access to any memory that is inside the Super NES, i.e., no access to the working RAM 32 or PPU video RAM 30.

The paragraph beginning at line 24, of page 28 through line 12 of page 29 has been amended as follows:

The Super NES video game machine which is represented in block form in Figure 2 has only been generally described herein. Further details regarding the Super NES including PPU 24 may, for example, be found in U.S. [application Serial No. 07/651,265] Patent No. 5,327,158,

issued July 5, 1994, entitled "Video Processing Apparatus [which was filed on April 10, 1991], which [application] patent has been expressly incorporated herein by reference. Still further details such as how information is transferred between the Super NES and the game cartridge may be found in U.S. [Application Serial No. 07/749,530, filed on August 26, 1991] Patent No. 5,291,189, issued March 1, 1994, entitled "Direct Memory Access Apparatus in Image Processing System and External Storage Device Used Therein" and in U.S. Application Serial No. 07/793,735, filed November 19, 1991, entitled, "Mosaic Picture Display Apparatus and External Storage Unit Used Therefor", which applications are incorporated herein by reference.

The paragraph beginning at line 22, of page 29 through line 4 of page 30 has been amended as follows:

Figure 3 shows a perspective view of an exemplary mechanical design for a game cartridge case 19 for housing the Mario chip and other cartridge structure shown in Figure 1. Similarly, Figure 3 shows the perspective view of an exemplary exterior housing for a video game control deck 20 for housing the Super NES video game hardware shown in Figure 2. The mechanical design for such video game control deck 20 and associated removable game cartridge 19 is shown in Figures 2-9 of U.S. [application Serial No. 07/748,938, filed on August 23, 1991] Patent No. 5,192,082, issued on March 9, 1993, entitled, "TV Game Machine", which [application] patent is hereby incorporated herein by reference.

In The Claims:

Claims 1-79 have been cancelled, without prejudice or disclaimer.

The following new claims 80-205 have been added.

--80. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising:

a programmable graphics processor;

a main processor that communicates information relating to one or more polygon-based 3D graphic objects to said programmable graphics processor,

wherein the graphics processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device.

81. A home video game system as in claim 80 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

82. A home video game system as in claim 80 wherein the graphics processor is a pipelined processor.

83. A home video game system as in claim 80 wherein the graphics processor is a programmable pipelined processor.

84. A home video game system as in claim 80 wherein the graphics processor includes embedded RAM cache memory.

85. A home video game system as in claim 80 wherein the graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

86. A home video game system as in claim 80 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

87. A home video game system as set forth in claim 86 wherein the multiplier performs multiply operations using at least 16-bit length operands.

88. A home video game system as in claim 80 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

89. A home video game system as in claim 80 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

90. A home video game system as in claim 80 wherein the graphics processor is programmed to perform texture mapping operations.

91. A home video game system as in claim 80 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

92. A home video game system as in claim 80 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

93. A home video game system as in claim 80 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

94. A home video game system as in claim 80 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

95. A home video game system as in claim 80 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

96. A home video game system as in claim 80 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

97. A home video game system as in claim 80 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

98. A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving removable memory, comprising:

a game program processing unit for executing at least a portion of a videographics program for displaying polygon-based 3D objects; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for rendering one or more portions of polygon-based 3D objects for display on said television type monitor display.

99. A home video game system as in claim 98 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

100. A home video game system as in claim 98 wherein the graphics processor is a pipelined processor.

101. A home video game system as in claim 98 wherein the graphics processor includes a high speed multiplier circuit.

102. A home video game system as in claim 98 wherein the graphics processor includes embedded RAM cache memory.

103. A home video game system as in claim 98 wherein the graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

104. A home video game system as in claim 98 wherein the graphics processor includes at least an Arithmetic Logic Unit and a plurality of registers for executing instructions for performing rotation and/or scaling of a polygon-based graphic object to be displayed.

105. A home video game system as in claim 98 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

106. A home video game system as set forth in claim 105 wherein the multiplier performs multiply operations using at least 16-bit length operands.

107. A home video game system as in claim 98 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

108. A home video game system as in claim 98 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

109. A home video game system as in claim 98 wherein the graphics processor is programmed to perform texture mapping operations.

110. A home video game system as in claim 98 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

111. A home video game system as in claim 98 having a set of instructions for programming the graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

112. A home video game system as in claim 98 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

113. A home video game system as in claim 98 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

114. A home video game system as in claim 98 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

115. A home video game system as in claim 98 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

116. A home video game system as in claim 98 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

117. A home video game system for use with a television type display device said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data, comprising:

a game program processor; and

a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, said graphics processor including a programmable processor having embedded RAM cache memory.

118. A home video game system as in claim 117 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

119. A home video game system as in claim 117 wherein the graphics processor is a pipelined processor.

120. A home video game system as in claim 117 wherein the graphics processor includes a high speed multiplier circuit.

121. A home video game system as in claim 117 wherein the graphics processor includes a plurality of data storage registers.

122. A home video game system as in claim 117 wherein the graphics processor includes graphic geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

123. A home video game system as in claim 122 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

124. A home video game system as set forth in claim 123 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

125. A home video game system as in claim 117 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

126. A home video game system as in claim 117 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

127. A home video game system as in claim 117 wherein the graphics processor is programmed to perform texture mapping operations.

128. A home video game system as in claim 117 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

129. A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

130. A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

131. A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

132. A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

133. A home video game system as in claim 117 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

134. A home video game system as in claim 117 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

135. A home video game system, for use with a television type monitor display device, said system having a housing and an insertion port in the housing for receiving removable program memory, comprising:

a game program processing unit for executing at least a portion of a videographics program for displaying polygon-based 3D graphic objects;

a video RAM for providing video frame data to a display device; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for subsequent transfer to said video RAM corresponding to one or more portions of polygon-based objects to be displayed.

136. A home video game system as in claim 135 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

137. A home video game system as in claim 135 wherein the graphics processor is a pipelined processor.

138. A home video game system as in claim 135 wherein the transfer of pixel data to video RAM is a direct memory assess (DMA) type transfer.

139. A home video game system as in claim 135 wherein the graphics processor includes a high speed multiplier circuit.

140. A home video game system as in claim 135 wherein the graphics processor includes embedded RAM cache memory.

141. A home video game system as in claim 135 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

142. A home video game system as in claim 135 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

143. A home video game system as set forth in claim 142 wherein the multiplier performs multiply operations using at least 16-bit length operands.

144. A home video game system as in claim 135 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

145. A home video game system as in claim 135 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

146. A home video game system as in claim 135 wherein the graphics processor is programmed to perform texture mapping operations.

147. A home video game system as in claim 135 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

148. A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

149. A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed

multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

150. A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

151. A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

152. A home video game system as in claim 135 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

153. A home video game system as in claim 135 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

154. A home video game system for use with a television type monitor display device comprising:

a housing including an insertion port that receives a removable memory storing video game program data/instructions;

a game program processor that executes at least a portion of a videographics game program which displays polygon-based 3D objects; and

a graphics processor that renders at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, the graphics processor including at least an Arithmetic Logic Unit and graphics geometry transformation circuitry for performing graphic transformation operations.

155. A home video game system as in claim 154 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

156. A home video game system as in claim 154 wherein the graphics processor is a pipelined processor.

157. A home video game system as in claim 154 wherein the graphics processor is a programmable pipelined processor.

158. A home video game system as in claim 154 wherein the graphics processor includes embedded RAM cache memory.

159. A home video game system as in claim 154 wherein the circuitry for accelerating 3D graphic special transformation operations includes a high speed multiplier for performing computations for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

160. A home video game system as in claim 154 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

161. A home video game system as set forth in claim 160 wherein the multiplier performs multiply operations using at least 16-bit length operands.

162. A home video game system as in claim 154 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

163. A home video game system as in claim 154 wherein two or more polygon-based graphic objects are displayed simultaneously.

164. A home video game system as in claim 154 wherein the graphics processor is programmed to perform texture mapping operations.

165. A home video game system as in claim 154 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

166. A home video game system as in claim 154 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

167. A home video game system as in claim 154 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

168. A home video game system as in claim 154 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

169. A home video game system as in claim 154 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

170. A home video game system as in claim 154 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

171. A home video game system as in claim 170 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

172. A home video game system for use with a television type monitor display device, said system having a housing and an insertion port in the housing for receiving removable memory and including a game program processor and a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, the graphics processor comprising:

a programmable pipelined processor having an Arithmetic Logic Unit;

a multiplier unit;

a cache RAM; and

a plurality of registers;

wherein the graphics processor performs at least rotation and/or scaling operations on said polygon based objects.

173. A home video game system as in claim 172 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

174. A home video game system as in claim 172 wherein the graphics processor includes hardware geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

175. A home video game system as set forth in claim 172 wherein the multiplier performs multiply operations using at least 16-bit length operands.

176. A home video game system as in claim 172 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

177. A home video game system as in claim 172 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

178. A home video game system as in claim 172 wherein the graphics processor is programmed to perform texture mapping operations.

179. A home video game system as in claim 172 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

180. A home video game system as in claim 172 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

181. A home video game system as in claim 172 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

182. A home video game system as in claim 172 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

183. A home video game system as in claim 172 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

184. A home video game system as in claim 172 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

185. A home video game system as in claim 184 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

186. In a home video game system having a housing and an insertion port in the housing for receiving a removable memory for storing a video game program, said system including a game program processor for executing at least a portion of a videographics program for displaying polygon-based 3D objects, a programmable graphics processor and a video RAM for providing video frame data to a television type monitor display device, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on the display device, comprising the steps of:

computing display screen position coordinates for a rotated and/or scaled polygon-based object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object to the video RAM.

187. A home video game system for use with a television type monitor display device, said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data, comprising:

a game program processor;

a graphics processor for rendering at least one or more portioning of a polygon-based 3D graphic object for displaying on the display device; and

a CD ROM reader device, wherein at least a portion of program instructions and/or graphics data used in rendering a 3D graphic object is accessed from a CD ROM.

188. A home video game system as in claim 187 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

189. A home video game system as in claim 187 wherein the graphics processor is a pipelined processor.

190. A home video game system as in claim 187 wherein the graphics processor includes a high speed multiplier circuit.

191. A home video game system as in claim 187 wherein the graphics processor includes a plurality of data storage registers.

192. A home video game system as in claim 187 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

193. A home video game system as in claim 192 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

194. A home video game system as set forth in claim 193 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

195. A home video game system as in claim 187 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

196. A home video game system as in claim 187 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

197. A home video game system as in claim 187 wherein the graphics processor is programmed to perform texture mapping operations.

198. A home video game system as in claim 187 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

199. A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

200. A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

201. A home video game system as in claim 187 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

202. In a home video game system having an insertion port for receiving removable memory for storing video game program data and/or instructions, said system including a game program processor and a programmable pipelined graphics processor, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on a raster scan type display device, comprising the steps of:

computing bit mapped display screen position object coordinates for a rotated and/or scaled polygon-based an object to be displayed; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object a video display RAM.

203. The method as in claim 202 wherein the writing of pixel information is accomplished via a direct memory access (DMA) operation.

204. In a home video game system, having a game program processor and a programmable graphics processor, the graphics processor having circuitry for increasing computational speed when processing 3D graphic geometric transformation operations, a method of producing 3D type graphics display effects utilizing rotated and/or scaled polygon-based objects, comprising the steps of:

providing said graphics processor with information relating at least in part to a polygon based graphic object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object a video display RAM.

205. The method as in claim 204 wherein the writing of pixel information is accomplished via a DMA operation.--

In the Abstract:

The original Abstract has been deleted and a substitute Abstract was attached on a separate sheet attached at the end of this amendment.

A fully user-programmable, graphics [microprocessor] processor is disclosed which is designed to be embodied in a removable external memory unit for connection with a host video game information processing system. In an exemplary embodiment, a video game system is described including a host video game system housing a game program processor and a pluggable video game cartridge [housing] containing the graphics [microprocessor] processor. [The game cartridge also includes a read-only program memory (ROM) and a random-access memory (RAM)]. The graphics [coprocessor] processor communicates with the host game processor and incorporates an embedded RAM cache memory. [operates in conjunction with a three bus architecture embodied on the game cartridge. The graphics processor using this bus architecture may execute programs from either the program ROM, external RAM or its own internal cache RAM.] The [fully user] programmable graphics [coprocessor] processor has hardware circuitry for performing 3D geometry transformations such as rotating and/or scaling polygon-based 3D graphic objects and also includes [an instruction set which is designed to

efficiently implement arithmetic operations associated with 3-D graphics and, for example, includes special instructions executed by] dedicated hardware for plotting individual pixels [in the host video game system's] for use with a character-mapped type display arrangement. [which, from the programmer's point of view, creates a "virtual" bit map by permitting the addressing of individual pixels -- even though the host system is character based. The graphics coprocessor interacts with the host coprocessor such that the graphics coprocessor's 16 general registers are accessible to the host processor at all times.] The graphics processor utilizes an instruction set that is designed to efficiently implement rotation and scaling operations associated with 3D graphics and includes special instructions for plotting character-mapped pixels.